with probable technological development in the future, five-time error correction for a DVD could be realized by providing five mid-term result registers, and that the process of EDCs could be greatly reduced in accordance with the degree of errors.

When there are only few errors in the second-time error correction, the third-time error correction can be canceled and only error detection can be executed.

In the pipeline processing shown in Figure 16 of the present embodiment, in order to improve throughput, data are stored in the buffer memory 4 in descending order of ECC blocks, and after the error correction, data are transferred downstream in descending order in unit time of the pipeline processing. Instead, some ECC blocks could be stored collectively in the buffer memory 4 (so-called batch processing) and after the error correction, some ECC blocks could be transferred downstream collectively in the descending order. This system is convenient for the case where access to the data-storing medium is often busy.

The system is also convenient when discrete scenes are reproduced at high speed in accordance with the predetermined procedure in order to retrieve specific images in a movie. In this case, it is necessary to provide a means compliant with the standard so as to recognize each scene and discrete scenes.

The system will be also convenient in the case where error correction is needed across several ECC blocks because a disk has a blemish or a stain while being handled by users, although probable technological development in the future will lessen error correction. Thus, most ECC blocks with few

error correction would be flown downstream as they are, and ECC blocks requiring minor error correction are collectively subjected to error correction, and when error correction is difficult, another process would be applied to collective ECC blocks.

(Embodiment 7)

While in Embodiment 6, error correction and error detection are performed in the first-time error correction for a code word temporarily stored in the buffer memory 4, in the present embodiment the first-time error correction and detection are performed in parallel with demodulation. In order to realize this feature, as shown in Figure 18, the error detection device of the present embodiment comprises two syndrome calculators and two error detectors. The error detection device will be described as follows with reference to Figure 18.

The drawing includes the first and second syndrome calculators 51 and 52, and the first and second error detectors 71 and 72. The upstream and downstream units are not illustrated.

The error detection device 100 receives data stored in an optical disk as a reception code 29 from the amplifier. The reception code 29 is entered to the demodulator 10. The demodulated code is stored in the buffer memory 4 by means of the demodulating code input signal 25 outputted from the bus control unit 3, and also supplied to the second syndrome calculator 52 and to the second error detector 72.

In order to perform error correction and error detection with the code word read from the buffer memory 4, the first syndrome calculator 51 and the first error detector 71 are arranged separately. The input of the error

corrector 61 is connected to a selection circuit 60 so that the error corrector 61 can select between the syndromes transmitted from the first and second syndrome calculators 51 and 52.

The second syndrome calculator 52 calculates a syndrome 162 of each transferred horizontal code word, and outputs the syndrome 162 to the error corrector 61. If the code word contains an error-containing code or if the syndrome 162 is not zero, the second syndrome calculator 52 outputs the error-containing code detection signal 222 to the second error corrector 72 and to the system control unit 1. The second syndrome calculator 52 also provides the system control unit 1 with an error-containing code word signal 232 indicating the code word from which an error has been detected.

The second error detector 72 executes an error detecting calculation for the transferred data in parallel with this.

When the second syndrome calculator 52 detects an error-containing code word, the error corrector 6 performs error correction, and the results are written in the buffer memory 4. Then, vertical error detection and correction and the second-time and later horizontal error detection and correction are executed by the first syndrome calculator 51 and the first error detector 71. Prior to the error detection, the mid-term results of the EDCs in the preceding code words stored in the mid-term result register assigned in the pipeline processing are reloaded. If the syndrome is zero when the transfer of the code words is over, the mid-term results of the EDCs are stored in the mid-term result register again. When the syndrome is not zero, on the other hand, the mid-term results of the EDCs in the preceding code words are maintained, without updating the contents